ISSN 2348 – 8034
Impact Factor- 3.155

GLOBAL JOURNAL OF ENGINEERING SCIENCE AND RESEARCHES

DESIGN OF LOW POWER ADJUSTABLE PULSE SHAPING FIR INTERPOLATOR FILTER

Mrs.N.Subbulakshmi*[1], N.Sahanaa sree[2], K.Naga Deepika3, T.Naga Lakshmi[4], G.S.Revathy[5]

*[1]Associate Professor,Department of ECE, Sri Ramakrishana Engineering College,Coimbatore,Tamilnadu, India.

[2,3,4,5]UG Scholar,Department of ECE, Sri Ramakrishana Engineering College, Coimbatore,Tamilnadu, India.

ABSTRACT

In this paper, a two step optimisation technique is proposed for designing a re-configurable VLSI architecture of an interpolation filter for multi-standard DIGITAL UP COUNTER (DUC) to reduce the power and area consumption. While designing a root-raised-cosine finite-impulse response filter for sub-filters DUC for three different standards, this technique initially reduces the number of multiplications per input sample and additions per input sample by 83% in comparison with individual implementation of each standard's filter. In the second step, a 2-bit binary common sub expression (BCS)-based BCS elimination algorithm has been proposed to design an efficient constant multiplier which is the basic element of any filter. This technique has succeeded in reducing the power and area usage by 38% and 41%, respectively.It also provides 36% improvement in operating frequency over a 3-bit BCS-based technique .It can be considered more appropriate for designing the multi-standard DUC. Index Terms-Digital up converter (DUC),FINITE IMPULSE RESPONSE (FIR) interpolation filter, reconfigurable hardware architecture, software defined radio (SDR) system.

Keywords: *Interpolator filter, Digital UP Counter (DUC) etc.*

I. INTRODUCTION

The different operating modes of the present day cell phones require various high data transfer rates and high channel capacities. This made the telecommunication industry to develop the concept of software defined radio (SDR). Under the wireless communication category, the present as well as upcoming standards can be supported by a single device known as SDR. In an SDR system, by providing a programmable channel select filter at the baseband level,sub-filters can be realized in a single chip. Different standards have different channel bandwidths, sampling rates, carrier-to-noise ratios, blocking, and interference profiles. The telecommunication industry of today is facing a major challenge with the development of a reconfigurable sample rate converter chip. Several researchers have contributed toward designing a low-power, low-area, and low-complexity reconfigurable channel filter for data rate conversion in SDR system. The reduction in power has been achieved by compromising with the speed of operation that makes balanced modular architecture, separate signed processing architecture and modified canonical signed digit(CSD) technique-based finite-impulse response(FIR) filter unsuitable for the SDR system.

When compared with the conventional FIR filter implementation, efficient use of LOOK UP TABLES(LUTs) in this model helps to reduce area and power. There is an increase in the ROM size in higher order filter implementation. Hence this architecture fails to achieve low power. The implementation of an area-delay-power efficient FIR filter by systolic decomposition of distributed arithmetic (DA)-based inner-product computation showed that reduction in memory size leads to increase in the area and latency. Based on modified DA technique, high-speed and medium-speed FIR filter architectures have been proposed in based on modified DA technique. Huge area is consumed when LUTs are working in parallel in a high-speed FIR filter design. This also draws a high current. To design the digital filter CSD based technique used in one novel digit serial reconfigurable FIR filter serves as a better solution rather than multiply and accumulate-based approach. In common sub-expression elimination (CSE) technique, multiplication between the constant coefficients and inputs are executed by shift and add operations .Since multiplication is repeated addition, the number of addition operations used to perform the multiplication defines the logic depth (LD) or the critical path of the circuit. But there were lower bound issues while performing constant multiplication(CM).While implementing higher order digital filters, it could be done with less hardware components with CSE algorithm.Based on binary CSE(BCSE) algorithm, a low-complexity architecture could be implemented with less power consumption and less hardware components than those of CSD-CSE method using programmable shift-and-add block. However, constant shift multiplication-based FIR filter architecture involves use of repeated

ISSN 2348 – 8034
Impact Factor- 3.155

adders in the multiplier block. In an SDR system low area and low power consumption is the main criteria. Because of redundant adders, this becomes unsuitable for SDR system. While designing a multi-standard Digital Up Converter (DUC) for SDR system ,more power and area can be reduced by using a low complexity multiplier. The multiplications per input sample(MPIS) , additions per input sample(APIS), hardware components, power can be reduced by overcoming disadvantages of existing reconfigurable architecture and by designing an efficient constant multiplier using 2-bit binary common subexpression (BCS).

II. ISSUES IN DESIGNING THE RECONFIGURABLE ROOT-RAISED-COSINE FIR FILTER AND ITS PROPOSED METHOD FOR SOLUTION .

Issues in Designing the Reconfigurable RRC FIR Filter for Sub-filters DUC. As a design example of Sub-filters DUC, we have considered three standards, namely universal mobile telecommunication system, wideband code division multiple access, and digital video broadcasting. These three standards have adopted root-raised-cosine (RRC) filter as the pulse shaping filter [14] for its ability to decrease the bit error rate by disallowing timing jitter at the sampling instant. The specifications of these standards presented in Table I are used to calculate the required filter lengths and the interpolation factors. The MATLAB analysis report for each filter is shown in Table I. Efficient hardware implementation of a reconfigurable RRC FIR interpolation filter with the specification mentioned in Table I throw up the following challenges. 1) For a filter ofN tap with interpolation factor of R,N/R equivalent multipliers (to implement the convolution operation between the inputs and the filter coefficients), and structural adders (to perform the final addition operation for generating the output) are required. Implementation of three different filter lengths of L, M, and N with three different interpolation factor P, Q, R would require L/PM/QN/Rnumber of equivalent multipliers and structural adders. Now, if the filter parameters (roll-off factors for RRC filter) are different, the total number of multipliers and structural adders will linearly increase with the number of parameters considered for design- ing the filter. For a constant propagation delay, the problem of area and power consumptions increases as the number of multipliers and structural adders increases for implementing the variable length higher order filter in a single architecture. 2) Amongst several techniques proposed earlier, the BCSE method is the recently proposed popular method for implementing an efficient constant multiplier. In BCSE algorithm, a coefficient of m-bit word length can form $2m - (m + 1)$ BCS amongst themselves. Proper choice of the length of the BCS is an important factor to avoid the inefficient utilization of hardware. 3) In BCSE technique, LD is the critical path that mainly depends on the number of addition operations in a chain. Propagation delay of the filter is measured by the computation time of (LD + 1) addition operations. Proper use of BCS to decrease the LD that maximizes the operating frequency of the filter is a challenge. 4) CMs are performed through shift and add operations. For example, if X is the number of adders required for a single CM operation, implementation of L-, M-, and N-tap filters will require$\{[L/2+M/2+N/2]* X\}$number of adders. By reducing the number of adders by Y say, for a single CM, one can save $\{[L/2+M/2+N/2]* Y\}$ number of adders to implement the desired reconfigurable FIR interpolation filter. Therefore, the task of maximizing the value of Y can pose a challenge to the designer.

III. EXISTING SYSTEM

In existing system a two-step optimization technique was used for designing a reconfigurable VLSI architecture of an interpolation filter for multi-standard digital up converter (DUC) to reduce the power and area consumption They initially reduces the number of multiplications per input sample and additions per input sample by 83% in comparison with individual implementation of each standard's filter while designing a root-raised-cosine finite-impulse response filter for multistandard DUC for three different standards. In the next step, a 2-bit binary common sub expression (BCS)-based BCS elimination algorithm has been proposed to design an efficient constant multiplier, which is the basic element of any filter. This technique has succeeded in reducing the area and power usage by 41% and 38%, respectively, along with 36% improvement in operating frequency over a 3-bit BCS-based technique reported earlier, and can be considered more appropriate for designing the multi-standard DUC.

IV. PROPOSED SYSTEM

In proposed system we used pulse shaping FIR decimation filter operation.An ADC samples the detected analog signal and feeds into the DDC processing chain. Optionally, in advanced systems, an initial frequency translation (to shift the center frequency from pass band to baseband), RF processing (for example, channel estimation and carrier recovery), and additional filtering (decimation) can be performed prior to the base down-conversion function. A mixer is used in combination with a vector of one or more sinusoids to channelize the signal, then each channel is filtered (to provide decimation and channel selectivity), and finally demodulated (or otherwise interpreted). This

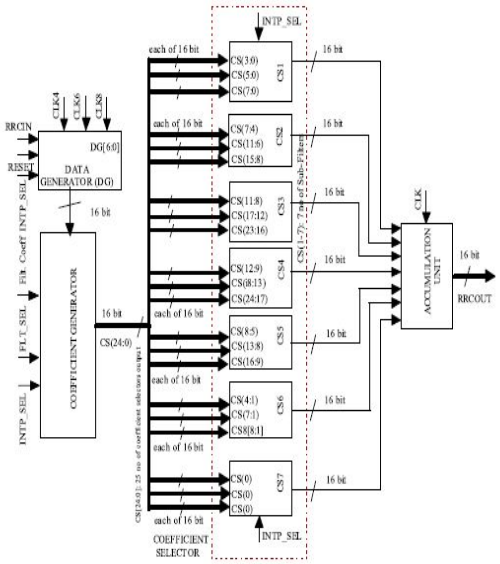
ISSN 2348 – 8034
Impact Factor- 3.155

application note covers the functions of the main mixer and filters (indicated by the red box in the diagram), with some reference to converters and demodulators. The optional functions are discussed briefly where relevant to provide some system context. Transmitting a signal at high modulation rate through a band-limited channel can create inter symbol interference. As the modulation rate increases, the signal's bandwidth increases. When the signal's bandwidth becomes larger than the channel bandwidth, the channel starts to introduce distortion to the signal. This distortion usually manifests itself as inter symbol interference. Not every filter can be used as a pulse shaping filter.

V. PROPOSED RECONFIGURABLE ARCHITECTURE

In this architecture, two parameters INTP_SEL and FLT_SEL are used to select different interpolation factors and roll-off factors, respectively. The master clock (CLK) that is used to sample the output (RRCOUT), operates at a higher rate than the other three clock sources CLK divided by four (CLK4), by six (CLK6) and by eight (CLK8), respectively, which have been used for sampling the serial input data (RRCIN) for different interpolation factors. The proposed reconfigurable RRC filter architecture consists of the major modules,data generator (DG), a coefficient generator (CG),a coefficient selector (CS), and an accumulation unit block (FA).

PROPOSED ARCHITECTURE OF THE RECONFIGURABLE RRC FILTER



A.DATA GENERATOR:

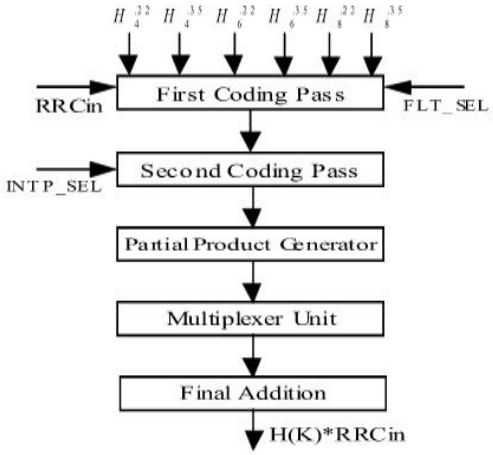
When the clock signal is applied to the data generator, the data has been mechanically furnished by sampling the input signal. The input data is sampled based on the selected value of the selection lines of multiplexer. It is used to sample the input data depending on the selected value of the decimation factor selection parameter.

B.CG BLOCK:

The CG block performs the multiplication between the inputs and the filter coefficients. The steps mention the previous section have been adopted to enable low area consumption and low complexity. Coefficient generator comprises of first coding pass, second coding pass, Partial Product Generator, multiplexer unit and addition.

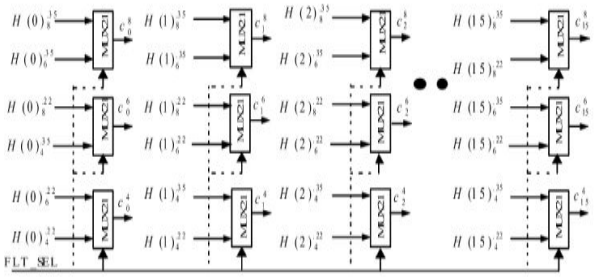
ISSN 2348 – 8034
Impact Factor- 3.155

DATA FLOW DIAGRAM OF PROPOSED CG BLOCK



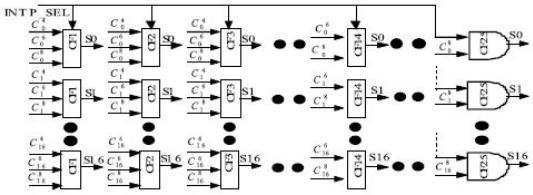
1) **FCP***:* In one FCP block, two sets of 25-, 27-, and 49-tapfilter coefficients differing only by roll-off-factor are the inputs.Inside the FCP block, three coding pass (CP) blocks are runningin parallel for three different interpolation factors. Occurrenceof matching between all bits is explored vertically between twocoefficients of same length filter.

ARCHITECTURE FOR IMPLEMENTATION OF FCP



2) **SCP:** The outputs from FCP block are three sets of coded coefficients that are 13, 19, and 25 in number and pass through another CP block to get the final coefficient set. In the SCP,
the common terms present vertically in between these three coded coefficient sets have been found out and coded accordingly.

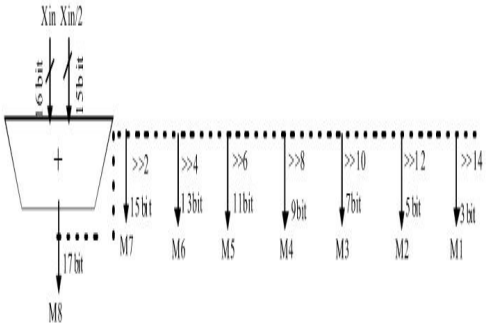
ARCHITECTURE OF IMPLEMENTATION OF SCP



3) **PARTIAL PRODUCT GENERATOR (PPG) Unit:** Shift-and-add method is used to generate the partial product during the multiplication operation between the input data (Xin) and the filter coefficients. In BCSE technique, realizations of the common subexpression using shift-and-add method eliminate the common term present in a coefficient. In the proposed architecture,2-bit BCSs ranging from 00 to 11 have been considered. Within four of these BCSs, an adder is required only for the pattern 11.This facilitates reduction in hardware and improvement in speed while performing the multiplication operation.

ISSN 2348 – 8034
Impact Factor- 3.155

ARCHITECTURE OF IMPLEMENTATION OF PPG

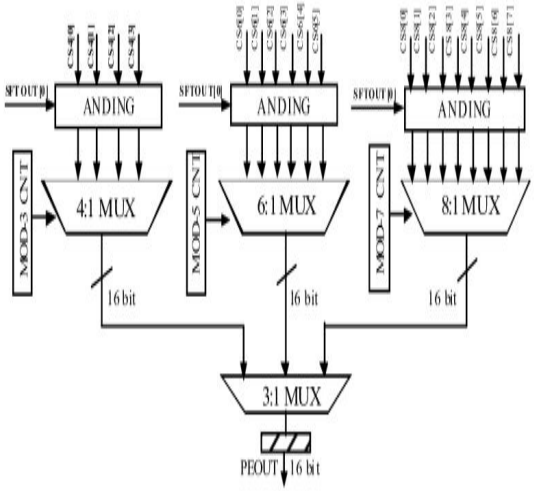


4) MULTIPLEXER UNIT: Depending on the coded coefficients, the multiplexer unit will select the appropriate data generated from the PPG unit. The BCS of length 2 bits would require eight4:1 multiplexer units to produce the partial product that will be added to perform the multiplication operation considering the coefficient word length of 16 bits each.

5) ADDITION UNIT: Addition unit performs the task of summing all the outputs of the PPG block followed by eight multiplexer units. Different word length adders are required for different binary weights. The outputs from the eight multiplexers M7–M0 are added together. The output of the final adder passes through a two's complementer circuit. The final output from this addition unit depends on the sign magnitude bit of the coded coefficient set

VI. C. COEFFICIENT SELECTOR

The Coefficient Selector takes the input from the output of the coefficient generator which selects the required data for processing. Then the selected inputs are simulated in AND logic to perform multiplication operation. In the proposed reconfigurable FIR filter, the CS block is used tosteer proper data to the final accumulation block depending on the corresponding interpolation factor parameter.



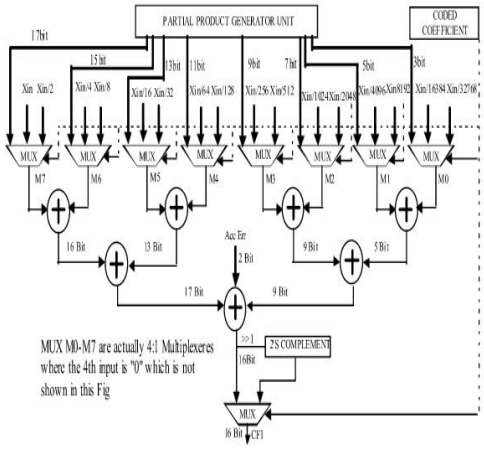
HARDWARE ARCHITECTURE OF CS BLOCK

ISSN 2348 – 8034
Impact Factor- 3.155

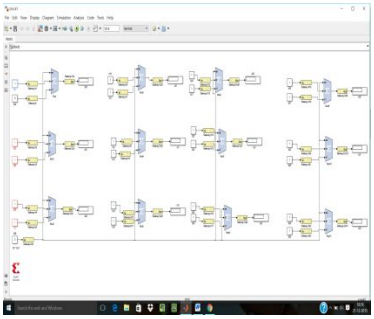
D. FINAL DATA ACCUMULATION UNIT(FA):

The inputs for accumulation were taken from the output of the data generator, coefficient generator and coefficient selector which are then added and the filter output will be produced. Depending on the coded coefficients, the multiplexer unit will select the appropriate data generated from the PPG unit. The proposed reconfigurable FIR filter is based on transposed direct form architecture. The final accumulation block has a chain of six adders and six registers as there is seven sub-filters.

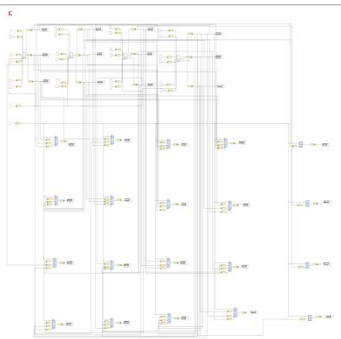
BLOCK DIAGRAM OF MULTIPLEXER AND FINAL ADDITION



VII. XILINX AND MATLAB OUTPUT

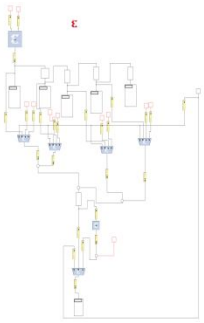


VII.1.FCP BLOCK OUTPUT.

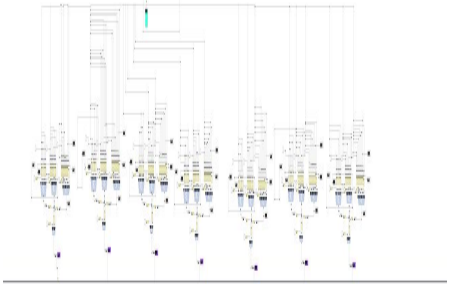


VII.2.FCP AND SCP OUTPUT

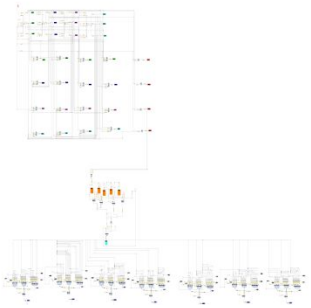
ISSN 2348 – 8034
Impact Factor- 3.155



VII.3.PPG AND MULTIPLEXER AND ADDITION UNIT BLOCK



VII.4.CS BLOCK



VII.5.ARCHITECTURE OF THE RRC

VIII. RESULTS AND DISCUSSION

The proposed design has been implemented onXC2V3000FF1152-4 Field-Programmable Gate Array (FPGA) device using Xilinx ISE 9.2i EDA tool. Comparisons have been done considering the 16-bit width of the input and the width of the coefficient varying by 8, 12, and 16 bits. Based on the trade off between area and delay, we have considered the area and delay product for a fair comparison.

COMPARISON RESULTS OF FPGA PLATFORM

References		Method Used	Filter Length	Max. Freq (MHz)	Slices (LUT)	Gate Count
Proposed	XC2VP4	2-bit BCSE	25/37/49 Tap 16X17	83.4	3,142	29,470
	XCV2000E			49.5	1,788	30,564
	XCV3000			58.9	1,742	29,425
	XC3S400N			69.74	1,749	29,545
[16] XC2VP4		MAC Based	64 Tap 16X16	59.7	9942	-
[6] XCV2000E		DA Based	64 Tap 8X8	64	1,061	23,878
[13] XCV3000		3-bit BCSE	20 Tap 16X17	37.2	-	22,956
[17] EP3C16Q		DA Based	32 Tap 8X8	93.69	1968	-

ISSN 2348 – 8034
Impact Factor- 3.155

COMPARISONS RESULTS FOR POWER CONSUMPTION

Prop. 16X16 [6] 8X8	Length	Clk Power (mW)	I/ P Power (mW)	Logic Power (mW)	O/P Power (mW)	Signal Power (mW)	Total Power (mW)
Prop.	16 Tap	13.04	11.14	68.33	102.3	36.40	231.21
[6]	16 Tap	25.65	1.41	83.75	61.12	64.37	236.3
Prop.	32 tap	18.66	11.14	74.98	102.3	40.28	247.36
[6]	32 Tap	42.6	1.41	169.86	64.18	108.66	386.71
Prop.	64 Tap	34.01	11.14	82.72	102.3	46.29	276.46
[6]	64 Tap	86.38	1.41	345.87	67.23	195.55	696.44

COMPARISONS OF DYNAMIC POWER CONSUMPTION

Ref	Tech (nm)	Power Supply	Length	Power (mW)	P(tap)
Our work	180	1.8V	49 Taps 16X16	17.46 @130 MHz	0.73
[8]	350	2.5 V	Eqv. 2.88 8X8	16.5 @86 MHz	19.03
[13]	180	1.8 V	20 Tap 16X16	7.8 @130 MHz	0.80
[20]	250	2.5V	75 Taps 16X16	653 @100 MHz	8.46

IX. CONCLUSION

This brief addresses the pulse shaping FIR filter for coming up with the reconfigurable filter used in multi-standard DUC, that is a crucial part of SDR/cognitive radio. This transient conjointly offers solutions to the issues to build the desired filter by reducing space and power together with improvement in frequency of the design. Comparisons of results of the planned design with alternative out there reconfigurable FIR filter designs enforced on FPGA similarly as ASIC platform demonstrate deserves of the planned architecture in terms of speed, power, and space consumption. The planned style appears to be remarkably appropriate for next generation multi-standard reconfigurable DUC of SDR system wherever power and space ought to be optimized.

REFERENCES

[1] J. Mitola, "The software radio architecture," IEEE Commun. Mag.,vol. 33, no. 5, pp. 26–38, May 1995.
[2] SDR Forum [Online]. Available: http://www.wirelessinnovation.org/what_is_sdr
[3] S. Im, W. Lee, C. Kim, Y. Shin, S. H. Lee, and J. Chung,"Implementation of SDR-eared digital IF channelized dechannelizer for multiple CDMA signals," IEICE Trans. Commun., vol. E83-B, no. 6,pp. 1282–1289, Jun. 2000.
[4] S.-F. Lin, S.-C. Huang, F.-S. Yang, C.-W. Ku, and L.-G. Chen,"Power-efficient FIR filter architecture design for wireless embedded system," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 51, no. 1,pp. 21–25, Jan. 2004.
[5] Y. Son, K. Ryoo, and Y. Kim, "1:4 interpolation FIR filter," IEEE Electron. Lett., vol. 40, no. 25, pp. 1570–1572, Dec. 2004.
[6] P. K. Meher, S. Chandrasekaran, and A. Amira, "FPGA realization of FIR filters by efficient and flexible systolization using distributed arithmetic," IEEE Trans. Signal Process., vol. 56, no. 7, pp. 3009–3017, Jul. 2008.
[7] J. Xie, J. He, and G. Tan, "FPGA realization of FIR filters for high-speed and medium-speed by using modified distributed arithmetic architectures," Microelectron. J., vol. 41, no. 6, pp. 365–371, Jun. 2010.
[8] K.-H. Chen and T.-D. Chieueh, "A low-power digit-based reconfigurable FIR filter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 8, pp. 617–621, Aug. 2006.
[9] O. Gustafsson, "Lower bounds for constant multiplication problems,"IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 11, pp. 974–978, Nov. 2007.
[10] D. Shi and Y. J. Yu, "Design of linear phase FIR filters with high probability of achieving minimum number of adders," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 1, pp. 126–136, Jan. 2011.
[11] Y. J. Yu and Y. C. Lim, "Optimization of linear phase FIR filters in dynamically expanding subexpressions space," Circuits, Syst., Signal Process., vol. 29. no. 1, pp. 65–80, 2010
[12] R. Mahesh and A. P. Vinod, "A new common subexpression elimination algorithm for realizing low-complexity higher order digital filters," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 2,pp. 217–229, Feb. 2008.
[13] R. Mahesh and A. P. Vinod, "New reconfigurable architectures for implementing FIR filters with low complexity," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 29, no. 2, pp. 275–288, Feb. 2010.

ISSN 2348 – 8034
Impact Factor- 3.155

[14] T. Acharya and G. J. Miao, "Square-root raised cosine symmetric filter for mobile communication," U.S. Patent 20 040 172 433, Sep. 2, 2004.
[15] Xilinx Inc., San Jose, CA, USA. (2014). Xilinx Logicore Multiplier IP version v9.0, [Online]. Available: http://www.xilinx.com/support/ documentation/white_papers/wp277.pdf
[16] J. Chandran, R. Kaluri, J. Singh, V. Owall, and R. Velijanovski, "Xilinx Virtex II Pro implementation of a reconfigurable UMTS digital channel filter," in Proc. IEEE Workshop Electron. Des., Test and Appl., Jan. 2004, pp. 77–82.
[17] S. F. Lin, S. C. Huang, F. S. Yang, C. W. Ku, and L. G. Chen, "Power-efficient FIR filter architecture design for wireless embedded system," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 51, no. 1, pp. 21–25, Jan. 2004.
[18] F. Sheikh, M. Miller, B. Richards, D. Markovic, and B. Nikolic, "A 1–190 MSample/s 8–64 tap energy-efficient reconfigurable FIR filter for multi-mode wireless communication," in Proc. IEEE Symp. VLSI\Circuits, Jun. 2010, pp. 207–208.
[19] S.-F. Hsiao, J.-H. Zhang Jian, and M.-C. Chen, "Low-cost FIR filter designs based on faithfully rounded truncated multiple constant multiplication/accumulation," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 60, no. 5, pp. 287–291, May 2013.
[20] S.-J. Lee, J.-W. Choi, S. W. Kim, and J. Park, "A reconfigurable FIR filter architecture to trade off filter performance for dynamic power consumption," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 12, pp. 2221–2228, Dec. 2011